

## **Amendments to the Claims:**

This following listing of claims will replace all prior versions, and listings, of claims in the application.

### **Listing of Claims:**

1. (original) A signal edge detector circuit having an output terminal and an input terminal for receiving microwave signals at a predetermined clock signal rate, said signal edge detector circuit comprising:

an input transmission line connected to said input and output terminals to provide a path for a signal transition from said input terminal to said output terminal, said input transmission line including a node between said input and output terminals;

a first reflection transmission line having first and second ends, said first reflection transmission line connected at a first end to said node providing a reflection of said signal transition, said reflection of a polarity to terminate said signal transition at said output terminal;

at least one second reflection transmission line having first and second ends, said at least one second reflection transmission line connected at a first end to said node providing a reflection of said signal transition, said reflection of a polarity to cancel out said reflection from said first reflection transmission line at said node;

whereby a pulse is generated at said output terminal for each leading signal edge of said microwave signals at said input terminal.

2. (original) The signal edge detector circuit of claim 1 wherein said first reflection transmission line is terminated by an open circuit; and said at least one second reflection transmission line is terminated by a first resistor connected to a reference voltage.

3. (original) The signal edge detector circuit of claim 2 wherein said voltage reference comprises ground.

4. (original) The signal edge detector circuit of claim 1 wherein said at least one second reflection transmission line is connected to said node through a second resistor; and said resistors connected to said at least one second reflection transmission line and

resistance/impedances of said input transmission line, said first reflection transmission line and said second reflection transmission line are selected with said input resistance/impedance and said load resistance/impedance so that a signal transition from said input terminal to said output terminal is terminated at said output terminal after a predetermined time interval and reflections of said signal transition back to said input terminal, to said first reflection transmission line and to said at least one second reflection transmission line are canceled.

5. (original) The signal edge detector circuit of claim 4 wherein said resistors connected to said at least one second reflection transmission line and said resistance/impedances of said input transmission line, said first reflection transmission line and said second reflection transmission line are further selected to match an input resistance/impedance at said input terminal and said load resistance/impedance at said output terminal.

6. (original) The signal edge detector circuit of claim 1 wherein said predetermined clock signal rate corresponds to a data stream rate of 40 Mb/sec.

7. (original) The signal edge detector circuit of claim 6 wherein said predetermined clock rate is 20 GHz/s.

8. (original) The signal edge detector circuit of claim 1 further comprising a second reflection transmission line connected in parallel to said at least one second reflection transmission line.

9. (currently amended) A clock signal generator for generating clock signals from a data stream at a predetermined clock rate from a microwave frequency system, said clock signal generator comprising:

a signal edge detector circuit having an output terminal and an input terminal connected to said microwave frequency system for receiving said data stream, said signal edge detector circuit comprising

an input transmission line connected to said input and output terminals to provide a path for each signal transition in said data stream from said input terminal to said output terminal, said input transmission line including a node between said input and output terminals;

a first reflection transmission line having first and second ends, said first reflection transmission line connected at a first end to said node providing a reflection of said signal transition, said reflection of a polarity to terminate said signal transition at said output terminal; and

at least one second reflection transmission line having first and second ends, said at least one second reflection transmission line connected at a first end to said node providing a reflection of said signal transition, said reflection of a polarity to cancel out said reflection from said first reflection transmission line at said node so that a pulse is generated at said output terminal for each leading signal transition of said data stream at said input terminal;

a ~~mixer~~ squaring circuit connected to said output terminal, said ~~mixer~~ squaring circuit producing a pulse train synchronous with said signal transitions in said data stream; and

a narrow-band filter receiving said pulse train to generate said clock signals at said predetermined clock rate.

10. (currently amended) The clock signal generator of claim 9 wherein said microwave frequency system comprises ~~an OC-768~~ a system which uses an OC-768 standard for signal transmission.

11. (original) The clock signal generator of claim 9 wherein said first reflection transmission line is terminated by an open circuit; and said at least one second reflection transmission line is terminated by a first resistor connected to a reference voltage.

12. (original) The clock signal generator of claim 11 wherein said voltage reference comprises ground.

13. (original) The clock signal generator of claim 9 wherein said at least one second reflection transmission line is connected to said node through a second resistor; and wherein said resistors connected to said at least one second reflection transmission line and

resistance/impedances of said input transmission line, said first reflection transmission line and said second reflection transmission line are selected with said input resistance/impedance and said load resistance/impedance so that said signal transition from said input terminal to said output terminal is terminated at said output terminal after a predetermined time interval and reflections of said signal transition back to said input terminal, to said first reflection transmission line and to said at least one second reflection transmission line are canceled.

14. (currently amended) The clock signal generator of claim 13 wherein said resistors connected to said at least one second reflection transmission line and said resistance/impedances of said input transmission line, said first reflection transmission line and said second reflection transmission line are further selected to match an input resistance/impedance of said microwave system at said input terminal and said load resistance/impedance of said squaring ~~mixer~~ circuit at said output terminal.

15. (original) The clock signal generator of claim 9 further comprising a second reflection transmission line connected in parallel to said at least one second reflection transmission line.

16. (original) A signal edge detector circuit having an output terminal and an input terminal for receiving microwave signals at a predetermined clock signal rate, said signal edge detector circuit comprising:

an input transmission line connected to said input and output terminals to provide a path for a signal pulse from said input terminal to said output terminal, said input transmission line including a node between said input and output terminals;

means connected to said node for providing a first reflection of said pulse, said reflection of a polarity to terminate said pulse at said output terminal;

means connected to said node for providing a second reflection of said pulse, said reflection of a polarity to cancel out said reflection from said first reflection transmission line at said node;

whereby a pulse is generated at said output terminal for each leading pulse edge of said microwave signals at said input terminal.